REMARKS/ARGUMENTS

This amendment is being filed contemporaneously with the RCE in response to the Final Office Action mailed January 25, 2005 ("*Final Office Action*"). Applicants note that in the *Final Office Action* claims 1-6, 9, 12-16 and 18 stand rejected. By this amendment, claims 1, 3-4, 6, 9 and 13-16 are amended and claims 22-29 are added. It is respectfully submitted that the pending claims define allowable subject matter.

Claims 1-6, 9, 12-16 and 18 stand rejected under 35 U.S.C. §102(a) as being anticipated by Wong, U.S. Patent No. 6,377,075 ("*Wong*"). Claims 1, 3-4, 6, 9 and 13-16 are amended. Applicants submit that the §102(a) rejection of claims 1-6, 9, 12-16 and 18 has been overcome.

It is well established that anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. As such, for an anticipation rejection, all of the elements and limitations of the claim must be found within a single prior art reference. Moreover, the Examiner bears the initial burden of establishing a *prima facie* case of anticipation.

The *Final Office Action* provides that *Wong* discloses:

> a circuit coupled to an output device (circuit of Figure 2), the circuit comprising at least one transistor device comprising at least one p-channel transistor device (M4), said at least one transistor device adapted to limit a duration of a high voltage across the output device thereby reducing hot carrier injection stress (see abstract).[1]

Applicants respectfully disagree.

Wong specifically discloses

> "a circuit topology for avoiding gate oxide-dielectric breakdown and hot carrier-degradation in circuits, such as CMOS inverters ... An inverter circuit according to the invention incorporates transistors M6, M2, M3, M5 appropriately biased, additional to those of a standard inverter circuit (comprising M1 and M4) in order to avoid hot-carrier degradation and gate-oxide breakdown of M4 and M1.[2]

In other words, *Wong* discloses an inverter circuit comprising six transistors M1, M2, M3, M4, M5 and M6 that avoids hot-carrier degradation and gate-oxide breakdown of a portion of the inverter circuit (i.e., a standard inverter circuit). *Wong* does not

[1] *Final Office Action*, page 2, lines 12-16.
[2] *Wong*, Abstract, lines 1-10.

disclose a circuit coupled to an output device or circuit, where the circuit reduces stress on the output device or circuit.

Specifically, *Wong* does not disclose "[a] circuit coupled to an output device... adapted to limit a duration of a high voltage across the output device thereby reducing hot carrier injection stress across the output device" as recited by amended claim 1, among other features; "[a]n integrated circuit...coupled to at least said output circuit and said IO PAD and adapted to limit a duration of a high voltage across said output circuit when said output circuit is enabled, thereby reducing stress on said output circuit" as recited by amended claim 9, among other features; "[a] method of controlling hot carrier injection stress comprising limiting a duration of a high voltage across an output device using a stress circuit...to limit said duration of said high voltage across said output device when said output device is enabled" as recited by amended claim 16, among other features; nor "[a] method of reducing stress across an output circuit...enabling the output circuit...dissipating a voltage across the output circuit; and preventing the output circuit from experiencing HCI stress" as recited by claim 18, among other features.

Additionally, the *Final Office Action* provides that with respect to claim 9, *Wong* discloses "an integrated circuit comprising: an I/O PAD (pad coupled to 15)..."[3] Applicants respectfully disagree. *Wong* does not disclose an "I/O PAD" as provided in the *Final Office Action*. Rather, Wong specifically discloses "input and output nodes 13,15"[4] In other words, *Wong* discloses separate input and outputs, and not the "I/O Pad" as recited by amended claim 9, among other features.

The *Final Office Action* further provides that with respect to claim 18, "the methods therein are inherent given the apparatus of Wong as shown in the above rejections."[5] Applicants disagree. Applicants note that *Wong* does not disclose tri-stating or a tri-stating circuit. Applicants respectfully submit that if *Wong* does not disclose tri-stating or a tri-stating circuit, it does not disclose "determining if the output circuit is tri-stated" as recited by claim 18, among other features.

As all the elements of independent claims 1, 9, 16 and 18 are not disclosed in a single reference, Applicants respectfully submit that such claims are allowable. Claims

---

[3] *Final Office Action*, page 2, lines 23-24 and page 3, line 1.
[4] *Wong*, col. 3, lines 33-34.

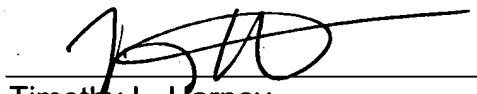
2-6 and 12-15 depend, directly or indirectly, from claims 1 and 9 respectively. Dependent claims 2-6 and 12-15 recite additional features and are believed allowable for all the reasons provided above with respect to claims 1 and 9.

New claims 22-25 depend from independent claim 18, recite additional features thereto and are believed allowable for all the reasons provided above with respect to claim 18. New claims 26-29 are similar in many respects to claims 1-6. Applicants submit that new claims 26-29 are allowable for the reasons provided above for claims 1-6.

In view of the foregoing, it is respectfully submitted that the pending claims define allowable subject matter, and Applicants respectfully request that the application be passed to issuance. Should the Examiner have any questions, he is invited to contact the undersigned at the telephone number listed below.

Dated: March 30, 2005

Respectfully submitted,



Timothy L. Harney
Reg. No. 38,174

McAndrews, Held & Malloy, Ltd.
500 West Madison Street
34th Floor
Chicago, IL 60661
Telephone: (312) 775-8000
Facsimile: (312) 775-8100

[5] *Final Office Action*, page 3, lines 11-12.